a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips;

a plurality of bonding wires for connecting said plural bonding pads to each other; and

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a via hole in said wiring layer, said via hole having a contact for connecting one of said plural bonding pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip,

wherein said second semiconductor chip is mounted on said wiring layer by an adhesive material and said wiring layer is provided on said first semiconductor chip without using an adhesive material.--

REMARKS

Claims 7-21 are present in the application. Claim 14 is amended to address the claim objection noted in the Official Action. Claims 8 and 14 are amended to address the 35 USC 112, second paragraph rejections noted in the Official Action.

Claims 7, 8, 12, 14, 15 and 17 stand rejected as anticipated by TAKIAR et al. 5,502,289.

Reconsideration and withdrawal of the rejection are respectfully requested because the reference does not disclose or suggest that a second semiconductor chip is mounted on a wiring layer by an adhesive material and the wiring layer is provided on a first semiconductor chip without using an adhesive material as

recited in each of independent claims 7, 12, 17 and 20 of the present application.

By way of example, Figures 3 and 4 of the present application show the second semiconductor chip 3 mounted on the wiring layer 8 by an adhesive material 4. However, the wiring layer 8 is provided on the first semiconductor chip 2 without using an adhesive material. The first semiconductor chip 2 can be connected to the wiring layer using a spin-coating method, for example. Removing the adhesive layer between the wiring layer 8 and the second semiconductor chip 2 reduces the number of manufacturing steps and also reduces the variation in the overall size of the semiconductor device by reducing the thickness of the device.

In contrast, TAKIAR et al. in Figure 7, for example, show first and second semiconductor chips 136 and 140 both connected to substrate material 138 using an adhesive material. Each of the figures of TAKIAR et al. show an adhesive layer connecting one layer (chip or wiring layer) to another. Accordingly, TAKIAR et al. do not disclose or suggest that a wiring layer is provided on a first semiconductor chip without using an adhesive material as recited in each of independent claims 7, 12, 17 and 20 of the present application.

As the reference does not disclose that which is recited, the anticipation rejection is not viable and should be withdrawn.

Claims 9, 13 and 19 are rejected as unpatentable over TAKIAR et al. in view of BEILSTEIN, Jr. et al. 5,567,654. This rejection is respectfully traversed.

BEILSTEIN Jr. et al. is cited for the teaching of a connection wire connecting bonding pads of one layer with bonding pads of another layer. BEILSTEIN Jr. et al. do not disclose or suggest what is recited in claims 7, 12 and 17. As set forth above, TAKIAR et al. does not disclose or suggest what is recited in claims 7, 12 and 17. Since claims 9, 13 and 19 depend from claims 7, 12 and 17, respectively, and further define the invention, the combination of references would not render obvious claims 9, 13 and 19.

Claims 10, 11, 16, 18 and 20 are rejected as unpatentable over TAKIAR et al. in view of TOKUDA et al. 5,870,289. This rejection is respectfully traversed.

TOKUDA et al. is cited for the teaching of a through-hole through a wiring layer. TOKUDA et al. do not disclose or suggest what is recited in claims 7, 12, 17 and 20. As set forth above, TAKIAR et al.do not disclose or suggest what is recited in claims 7, 12, 17 and 20. Since claims 10, 11, 16, 18 and 20 depend from one of claims 7, 12, 17 and 20 and further define the invention, the combination of references would not render obvious claims 10, 11, 16, 18 and 20.

Claim 21 is rejected as unpatentable over TAKIAR et al. in view of TOKUDA et al. and further in view of BEILSTEIN Jr. et al. This rejection is respectfully traversed.

As noted above, BEILSTEIN Jr. et al. is cited for the teaching of a connection wire connecting bonding pads of one layer with bonding pads of another layer and do not disclose or suggest what is recited in claim 20. As set forth above, TAKIAR et al. in view of TOKUDA et al. do not disclose or suggest what is recited in claim 20. Since claim 21 depends from claim 20 and further defines the invention, the combination of references would not render obvious claim 21.

The above-noted features of claims 7, 12, 17, and 20 are missing from each of the references, are absent from the combination, and thus are not obvious to one having ordinary skill in the art.

Accordingly, it is believed that the claims avoid the rejections under §102 and §103 and are allowable over the art of record.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

Attached hereto is a marked-up version of the changes

made to the claims. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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"VERSION WITH MARKINGS TO SHOW CHANGES MADE."

The claims have been amended as follows:

--7. (amended) A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first semiconductor chip;

a wiring layer between said first and second semiconductor chips, said wiring layer including a polyimide tape having a copper foil layer therein;

a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips; and

a plurality of bonding wires for connecting said plural bonding pads to each other,

wherein said second semiconductor chip is mounted on said wiring layer by an adhesive material and said wiring layer is provided on said first semiconductor chip without using an adhesive material.

--8. (amended) The semiconductor device according to claim 7, wherein,

a first bonding wire connects one of said plural bonding pads on said substrate to one of said plural bonding pads

on said first semiconductor chip;

a second bonding wire connects one of said plural bonding pads on said substrate to one of said plural bonding pads on said wiring layer; and

a third bonding wire connects said one of said plural bonding pads on said wiring layer to one of said plural bonding pads on said [second] semiconductor substrate.

--12. (amended) A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first semiconductor chip;

a wiring layer between said first and second semiconductor chips, said wiring layer including a conductor within said wiring layer;

a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips; and

a plurality of bonding wires for connecting said plural bonding pads to each other,

wherein said second semiconductor chip is mounted on said wiring layer by an adhesive material and said wiring layer is provided on said first semiconductor chip without using an adhesive material.

--14. (amended) The semiconductor device according to claim 12, wherein

a first bonding wire connects one of said plural bonding pads on said substrate to one of said plural bonding pads on said first semiconductor chip;

a second bonding wire connects one of said plural bonding pads on said substrate to one of said plural bonding pads on said wiring layer; and

a third bonding wire connects another one of said plural bonding pads on said wiring layer to one of said plural bonding pads on said [second] semiconductor substrate,

said second and third [boding] bonding wire being electrically connected through said conductor.--

--17. (amended) A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first semiconductor chip;

a wiring layer between said first and second semiconductor chips, said wiring layer including a conductor traversing said wiring layer;

a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips; and

a plurality of bonding wires for connecting said plural bonding pads to each other,

wherein said second semiconductor chip is mounted on said wiring layer by an adhesive material and said wiring layer is provided on said first semiconductor chip without using an adhesive material.--

--20. (amended) A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first semiconductor chip;

a wiring layer between said first and second semiconductor chips, said wiring layer including a polyimide tape having a copper foil layer therein;

a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips;

a plurality of bonding wires for connecting said plural bonding pads to each other; and

a via hole in said wiring layer, said via hole having a contact for connecting one of said plural bonding pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip,

wherein said second semiconductor chip is mounted on said wiring layer by an adhesive material and said wiring layer is provided on said first semiconductor chip without using an adhesive material.--